NOTICE OF REVISION (NOR)

THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.

1. DATE *(YYMMDD)*	*Form Approved OMB No. 0704-0188*
99-06-01	

PLEASE DO NOT RETURN YOUR COMPLETED FORM TO EITHER OF THESE ADDRESSED. RETURN COMPLETED FORM TO THE GOVERNMENT ISSUING CONTRACTING OFFICER FOR THE CONTRACT/ PROCURING ACTIVITY NUMBER LISTED IN ITEM 2 OF THIS FORM.

2. PROCURING ACTIVITY NO.	
3. DODAAC	

4. ORIGINATOR	b. ADDRESS *(Street, City, State, Zip Code)*	5. CAGE CODE	6. NOR NO.
	Defense Supply Center Columbus 3990 East Broad Street Columbus, OH 43216-5000	67268	5962-R066-99
a. TYPED NAME *(First, Middle Initial, Last)*		7. CAGE CODE 67268	8. DOCUMENT NO. **5962-95635**

9. TITLE OF DOCUMENT	10. REVISION LETTER		11. ECP NO.
MICROCIRCUIT, DIGITAL, 16-BIT MICROCONTROLLER, RADIATION HARDENED, MONOLITHIC SILICON	a. CURRENT C	b. NEW D	N/A

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add “D”.
Revisions description column; add “Changes in accordance with NOR 5962-R066-99”.
Revisions date column; add “99-06-01”.
Revision level block; change from “C” to “D”.
Rev status of sheets; for sheet 1, change from “C” to “D”. For sheets 4 and 28 through 33, add “D”.

Sheets 4: Add new paragraph as follows: “3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.”
Revision level block; add “D”.

Sheets 28 through 33: Add attached appendix A.

Continued on next sheets.

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. *(X one)*		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	c. TYPED NAME *(First, Middle Initial, Last)*
DSCC-VAC	Monica L. Poelking

d. TITLE	e. SIGNATURE	f. DATE SIGNED *(YYMMDD)*
Chief, Custom Microelectronics Team	Monica L. Poelking	99-06-01

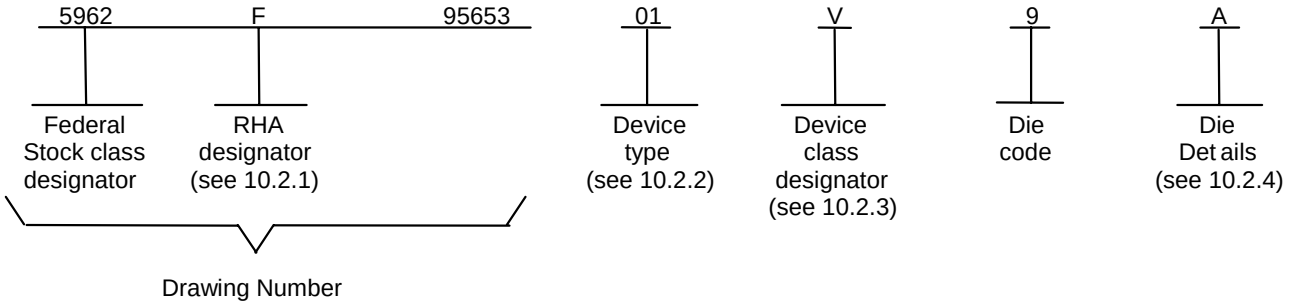
15a. ACTIVITY ACCOMPLISHING REVISION	b. REVISION COMPLETED *(Signature)*	c. DATE SIGNED *(YYMMDD)*
DSCC-VAC	Thanh V. Nguyen	99-06-01

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-95635

10. SCOPE

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

10.2 PIN. The PIN shall be as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS-RTX2010RH	16-bit microcontroller radiation hardened, SOS

10.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535.

10.2.4 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.4.1 Die Physical dimensions.

Die Types	Figure number
01	A-1

10.2.4.2 Die Bonding pad locations and Electrical functions.

Die Types	Figure number
01	A-1

10.2.4.3 Interface Materials.

Die Types	Figure number
01	A-1

10.2.4.4 Assembly related information.

Die Types	Figure number
01	A-1

10.3 Absolute maximum ratings. See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions. See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS

20.1 Government specifications, standards, bulletin, and handbooks. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-103 – List of Standard Microcircuit Drawings (SMD's).

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

20.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

30. REQUIREMENTS

30.1 Item Requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die Physical dimensions. The die physical dimensions shall be as specified in 10.2.4.1 and on figure A-1.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.4.2 and on figure A-1.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.4.3 and on figure A-1.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.4.4 and figure A-1.

30.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined within paragraph 3.2.4 of the body of this document.

30.3 Electrical performance characteristics and post- irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

30.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer Lot acceptance for Class V product using the criteria defined within MIL-STD-883 TM 5007.

b) 100% wafer probe (see paragraph 30.4).

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 TM2010 or the alternate procedures allowed within MIL-STD-883 TM5004.

40.3 Conformance inspection.

40.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified within paragraphs 4.4.4.1, 4.4.4.1.1, and 4.4.4.2.

50. DIE CARRIER

50.1 Die carrier requirements. The requirements for the die carrier shall be in accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

60. NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0674.

60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined with MIL-PRF-38535 and MIL-STD-1331.

60.4 Sources of Supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-95635

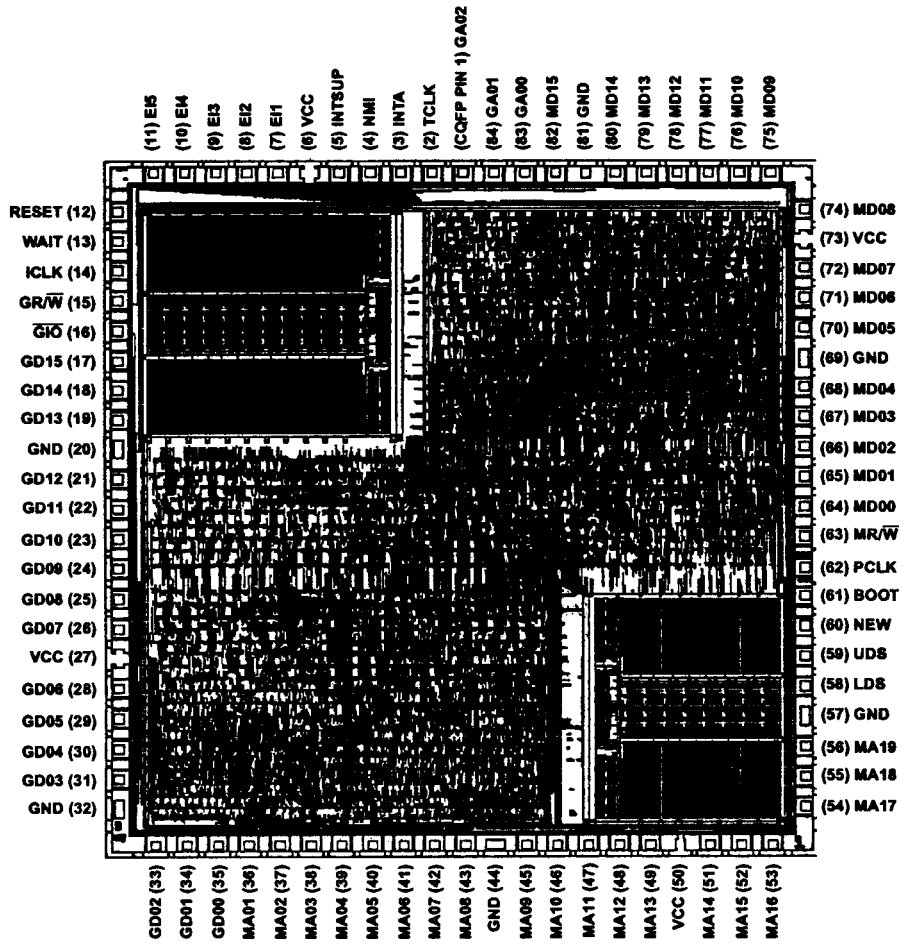
FIGURE A-1

o DIE PHYSICAL DIMENSIONS

Die Size:	9240 x 9530 microns.
Die Thickness:	21 ±2 mils.

o DIE BONDING PAD LOCATIONS AND ELECTRICAL FUNCTIONS

The following metallization diagram supplies the locations and electrical functions of the bonding pads. The internal metallization layout and alphanumeric information contained within this diagram may or may not represent the actual circuit defined by this SMD.



NOTE: Pad numbers reflect terminal numbers when placed in case outline Y (see figure 1).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-95635

o INTERFACE MATERIALS

Metal 1:	AlSi	7.0kA ±1kA
Metal 2 (Top):	AlSi	10.0kA ±1kA
Backside Metallization	None	
Glassivation		
Type:	PSG	
Thickness	13kA ±1.5kA	
Substrate:	Silicon on Sapphire (SOS)	

o ASSEMBLY RELATED INFORMATION

Substrate Potential: Insulator.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99-06-01

Approved sources of supply for SMD 5962-95635 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962F9563501V9A	34371	HS0-RTX2010RH-Q

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Harris Semiconductor P.O. Box 883 Melbourne, FL 32902-0883

NOTICE OF REVISION (NOR)

THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.

1. DATE *(YYMMDD)* 98-11-10

Form Approved OMB No. 0704-0188

2. PROCURING ACTIVITY NO.

3. DODAAC

4. ORIGINATOR	b. ADDRESS *(Street, City, State, Zip Code)*	5. CAGE CODE	6. NOR NO.
	Defense Supply Center Columbus 3990 East Broad Street Columbus, OH 43216-5000	67268	5962-R014-99
a. TYPED NAME *(First, Middle Initial, Last)*		7. CAGE CODE 67268	8. DOCUMENT NO. **5962-95635**

9. TITLE OF DOCUMENT	10. REVISION LETTER		11. ECP NO.
MICROCIRCUIT, DIGITAL, 16-BIT MICROCONTROLLER, RADIATION HARDENED, MONOLITHIC SILICON	a. CURRENT B	b. NEW C	N/A

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "C".
Revisions description column; add "Changes in accordance with NOR 5962-R014-99".
Revisions date column; add "98-11-10".
Revision level block; change from “B” to "C".
Rev status of sheets; for sheets 1 and 5, change from “B” to “C”. For sheet 21, add "C".

Sheet 5: Table I, Low output voltage, V_{OL}, conditions column; change I_{OL} from “4.0 V” to “4.0 mA”

Table I, Input leakage current, I_I, pre-irradiation limits; change from “-1.0 µA Min.” to “-5.0 µA Min.” and from “1.0 µA Max.” to “5.0 µA Max.” for subgroups 1 and 3. Change from “-5.0 µA Min.” to “-10.0 µA Min.” and from “5.0 µA Max.” to “10.0 µA Max.” for subgroup 2. Post-irradiation limits; change from “-5.0 µA Min.” to “-10.0 µA Min.” and from “5.0 µA Max.” to “10.0 µA Max.” for subgroup 1.

Table I, Standby power suppy current, I_{CCSB}, pre-irradiation limits; change from “500 µA Max.” to “3.0 mA Max.” for subgroups 1 and 3.
Revision level block; change from “A” to "C".

Sheet 21: Table IIA, Interim electrical parameters; delete subgroup 9 for device classes M, Q, and V.
Revision level block; add "C".

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. *(X one)*		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	c. TYPED NAME *(First, Middle Initial, Last)*
DSCC-VAC	Monica L. Poelking

d. TITLE	e. SIGNATURE	f. DATE SIGNED *(YYMMDD)*
Chief, Custom Microelectronics	Monica L. Poelking	98-11-10

15a. ACTIVITY ACCOMPLISHING REVISION	b. REVISION COMPLETED *(Signature)*	c. DATE SIGNED *(YYMMDD)*
DSCC-VAC	Thanh V. Nguyen	98-11-10

NOTICE OF REVISION (NOR)

This revision described below has been authorized for the document listed.

1. DATE: 96-04-23

Form Approved OMB No. 0704-0188

2. PROCURING ACTIVITY NO.

3. DODAAC

4. ORIGINATOR

a. TYPED NAME (First, Middle Initial, Last)

b. ADDRESS (Street, City, State, Zip Code)
Defense Electronics Supply Center
1507 Wilmington Pike
Dayton, OH 45444-5765

5. CAGE CODE: 67268

6. NOR NO.: 5962-R118-96

7. CAGE CODE: 67268

8. DOCUMENT NO.: 5962-95635

9. TITLE OF DOCUMENT
MICROCIRCUIT, DIGITAL, 16-BIT MICROCONTROLLER, RADIATION HARDENED, MONOLITHIC SILICON

10. REVISION LETTER
a. CURRENT: A
b. NEW: B

11. ECP NO.: N/A

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "B".
Revisions description column; add "Changes in accordance with NOR 5962-R118-96".
Revisions date column; add "96-04-23".
Revision level block; add "B".
Rev status of sheets; for sheets add "B".

Sheet 6. Change ICLK period (t_1) from: 62 ns Min to: 75 ns Min.

Change ICLK low time (t_3) from: 24 ns Min to: 32 ns Min.

Change status of Revision Level to "B".

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. (X one)		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT: DESC-ELDC

c. TYPED NAME (First, Middle Initial, Last): Monica L. Poelking

d. TITLE: Chief, Custom Microelectronics

e. SIGNATURE: Monica L. Poelking

f. DATE SIGNED (YYMMDD): 96-04-23

15a. ACTIVITY ACCOMPLISHING REVISION: DESC-ELDC

b. REVISION COMPLETED (Signature): Thomas M. Hess

c. DATE SIGNED (YYMMDD): 96-04-23

NOTICE OF REVISION (NOR)

This revision described below has been authorized for the document listed.

1. DATE (YYMMDD)	Form Approved OMB No. 0704-0188
95-12-18	

2. PROCURING ACTIVITY NO.
3. DODAAC

4. ORIGINATOR	b. ADDRESS (Street, City, State, Zip Code)	5. CAGE CODE	6. NOR NO.
	Defense Electronics Supply Center 1507 Wilmington Pike Dayton, OH 45444-5765	67268	5962-R020-96
a. TYPED NAME (First, Middle Initial, Last)		7. CAGE CODE 67268	8. DOCUMENT NO. 5962-95635

9. TITLE OF DOCUMENT	10. REVISION LETTER		11. ECP NO.
	a. CURRENT	b. NEW	
MICROCIRCUIT, DIGITAL, 16-BIT MICROCONTROLLER, RADIATION HARDENED, MONOLITHIC SILICON	Initial	A	

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "A".
Revisions description column; add "Changes in accordance with NOR 5962-R020-96"
Revisions date column; add "95-12-18".
Revision level block; add "A".
Rev status of sheets; For sheets 1, 5, and 9 add "A".

Sheet 5: Table I: Standby power supply current I_{CCSB}, subgroup 2 pre-irradiation and subgroup 1 post irradiation: delete "3.5 mA Max" and substitute "15.0 mA Max".
Table I: Operating power supply current I_{CCOP}, delete "35 mA Max" and substitute "40 mA Max".
Revision level block; add "A".

Sheet 9. Delete footnote 5/ and replace as follows: "5/ I_{CCOP} increases with frequency at approximately 5 mA/MHz."
Revision level block; add "A".

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. (X one)		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	c. TYPED NAME (First, Middle Initial, Last)
DESC-ELDC	Monica L. Poelking

d. TITLE	e. SIGNATURE	f. DATE SIGNED (YYMMDD)
Chief, Custom Microelectronics	Monica L. Poelking	95-12-18

15a. ACTIVITY ACCOMPLISHING REVISION	b. REVISION COMPLETED (Signature)	c. DATE SIGNED (YYMMDD)
DESC-ELDC	Larry T. Gauder	95-12-18

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27						

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Thomas M. Hess

CHECKED BY
Thomas M. Hess

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
95-09-27

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, 16-BIT MICROCONTROLLER, RADIATION HARDENED, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-95635

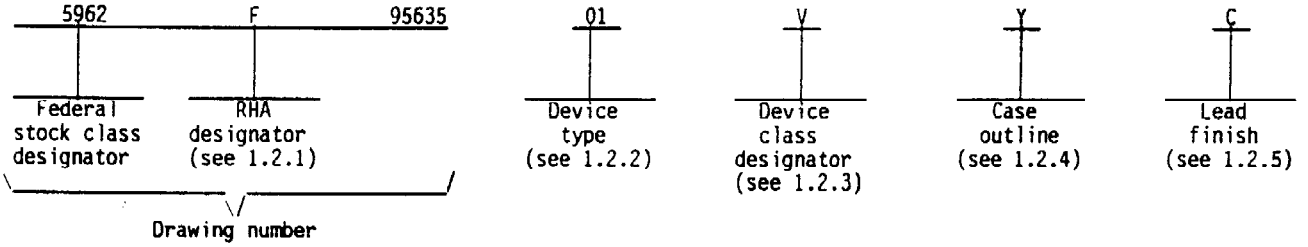
SHEET 1 OF 27

DESC FORM 193
JUL 94

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS-RTX2010RH	16-bit microcontroller radiation hardened, SOS

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA3-P85	85	Pin grid array
Y	See figure 1	84	Ceramic quad flat package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage	+6.0 V
Input, Output I/O voltage applied	GND - 0.3 V to VDD + 0.3 V
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+175°C
Lead temperature (solder 10 seconds)	+300°C
Thermal resistance, Junction-to-case (θ_{JC})	
Case X	3°C/W
Case Y	4°C/W
Thermal resistance, Junction-to-Ambient (θ_{JA})	
Case X	29°C/W
Case Y	34°C/W
Maximum power dissipation	2.0 W

1.4 Recommended operating conditions.

Operating supply voltage range	+4.5 V to +5.5 V
Operating temperature range	-55°C to +125°C
Maximum rise and fall time	5 ns max
Radiation features	
Total Dose	300K RAD(SI)
Single event phenomenon (SEP) effective	
Linear energy threshold (LET), No upset	> 100 MeV/(cm^2/mg) 2/
Dose rate upset (20 ns pulse)	> 1 x 10^{11} Rads (SI)/s 2/
Latch up	None 2/
Dose rate survivability	> 1 x 10^{12} Rads (SI)/s 2/
Cosmic ray upset immunity	< 1 x 10^{-10} Errors/Bit-Day 2/3/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Guaranteed by design or process but not tested.
3/ Single event upset error rates are obtained useing Adams 10% worst case environment under worst case conditions for upset.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified on table III.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/ 2/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input high voltage	V_{IH}	V_{DD} = 5.5 V 3/	1, 2, 3	01	$0.7V_{DD}$		V
Input low voltage	V_{IL}	V_{DD} = 4.5 V 3/	1, 2, 3	01		0.8	V
High output voltage	V_{OH1}	V_{DD} = 4.5 V, I_{OH} = -4.0 mA	1, 2, 3	01	3.5		V
High output voltage	V_{OH2}	V_{DD} = 4.5 V, I_{OH} = -100 µA	1, 2, 3	01	V_{DD} -0.4		V
Low output voltage	V_{OL}	V_{DD} = 4.5 V, I_{OL} = 4.0 V	1, 2, 3	01		0.4	V
Input leakage current	I_I	V_{DD} = 5.5 V, V_{IN} = 0 V or V_{DD}	1, 3	01	-1.0	1.0	µA
			2		-5.0	5.0	
		M, D, L, R, F	1		-5.0	5.0	
I/O leakage current	I_{IO}	V_{DD} = 5.5 V, V_{IN} = 0 V or V_{DD}	1, 2, 3	01	-10.0	10.0	µA
Standby power supply current	I_{CCSB}	V_{IN} 4/ = V_{DD} or 0 V, V_{DD} = 5.5V	1, 3	01		500	µA
			2			3.5	mA
		M, D, L, R, F	1			3.5	
Operating power supply current	I_{CCOP}	V_{IN} = V_{DD} or 0 V, V_{DD} = 5.5V ICLK = 1MHz 5/	1, 2, 3	01		35	mA
Input capacitance	C_{IN}	See 4.4.1c	4	01		20	pF
Output capacitance	C_{OUT}	See 4.4.1c	4	01		20	pF
Functional test		See 4.4.1b	7, 8	01			

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/ 2/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLOCK WAIT AND TIMER TIMING REQUIREMENTS							
ICLK period	t_1	3/	9, 10, 11	01	62		ns
ICLK high time	t_2	3/	9, 10, 11	01	24		ns
ICLK low time	t_3	3/	9, 10, 11	01	24		ns
Wait setup time	t_4	6/	9, 10, 11	01	5		ns
Wait hold time	t_5	6/	9, 10, 11	01	5		ns
EI high to EI high	t_6	External clock/timer input 3/	9, 10, 11	01	t_1x4		ns
EI high time	t_7	3/	9, 10, 11	01	20		ns
EI low time	t_8	3/	9, 10, 11	01	15		ns
CLOCK, WAIT AND TIMER TIMING RESPONSES							
ICLK to TCLK high	t_{11}		9, 10, 11	01	5	35	ns
TCLK low time	t_{12}	7/	9, 10, 11	01	52		ns
TCLK high time	t_{13}		9, 10, 11	01	55		ns
ICLK to PCLK high	t_{15}		9, 10, 11	01	5	35	ns
PCLK low time	t_{16}	7/ 8/	9, 10, 11	01	55		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/ 2/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLOCK, WAIT AND TIMER TIMING RESPONSES - continued							
PCLK high time	t_{17}		9, 10, 11	01	55		ns
ICLK to TCLK low	t_{19}		9, 10, 11	01		36	ns
ICLK to PCLK low	t_{20}		9, 10, 11	01		35	ns
MEMORY BUS TIMING REQUIREMENTS							
MD setup time	t_{21}	Read cycle 6/	9, 10, 11	01	25		ns
MD hold time	t_{22}	6/	9, 10, 11	01	4		ns
MEMORY BUS TIMING RESPONSES							
PCLCK to MA valid	t_{26}	9/	9, 10, 11	01		62	ns
MA hold time	t_{28}	9/	9, 10, 11	01	20		ns
PCLK to MR/$\overline{W}$ UDS, LDS, NEW, and BOOT valid	t_{29}	9/	9, 10, 11	01		50	ns
MR/$\overline{W}$ UDS, LDS, NEW, and BOOT hold time	t_{31}	9/	9, 10, 11	01	20		ns
PCLK to MD valid	t_{32}	Write cycle	9, 10, 11	01		20	ns
MD hold time	t_{33}	Write cycle 9/	9, 10, 11	01	20		ns
MD enable time	t_{34}	Write cycle	9, 10, 11	01	-3		ns
PCLK to MD disable time	t_{35}	Write cycle 9/	9, 10, 11	01		60	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/ 2/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ASIC BUS INTERRUPT TIMING REQUIREMENTS							
GD read setup to PCLK	t_{40A}	Read cycle not streamed 6/	9, 10, 11	01	55		ns
GD read setup to PCLK	t_{40B}	Read cycle streamed mode 6/	9, 10, 11	01	28		ns
GD read setup to $\overline{G1O}$	t_{41A}	Read cycle not streamed 6/	9, 10, 11	01	60		ns
GD read setup to $\overline{G1O}$	t_{41B}	Read cycle streamed mode 6/	9, 10, 11	01	33		ns
GD read hold from $\overline{G1O}$	t_{42}	Read cycle 6/	9, 10, 11	01	0		ns
GD read hold from PCLK	t_{43}	Read cycle 6/	9, 10, 11	01	0		ns
EINMI setup time	t_{44}	INT/NMI 6/	9, 10, 11	01	40		ns
INTSUP setup time	t_{46}	6/	9, 10, 11	01	22		ns
INTSUP hold time	t_{47}	6/	9, 10, 11	01	0		ns
ASIC BUS AND INTERRUPT TIMING RESPONSES							
PCLK high to $\overline{G1O}$ low	t_{48}	7/	9, 10, 11	01	52		ns
$\overline{G1O}$ low time	t_{49}	7/ 10/	9, 10, 11	01	52		ns
ICLK high to $\overline{G1O}$ low	t_{50}		9, 10, 11	01		43	ns
ICLK high to $\overline{G1O}$ high	t_{51}		9, 10, 11	01		40	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/ 2/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ASIC BUS INTERRUPT TIMING RESPONSES - continued							
PCLK to GA valid	t_{52}	9/	9, 10, 11	01		49	ns
$\overline{G1O}$ to GA hold time	t_{54}	9/	9, 10, 11	01	12		ns
PCLK to GR/$\overline{W}$ valid	t_{56}	9/	9, 10, 11	01		50	ns
$\overline{G1O}$ to GR/$\overline{W}$ hold time	t_{58}	9/	9, 10, 11	01	15		ns
GD enable time	t_{61}	Write cycle	9, 10, 11	01	-7		ns
GD valid time	t_{62}		9, 10, 11	01		16	ns
$\overline{G1O}$ to GD hold time	t_{63}	Write cycle 9/	9, 10, 11	01	12		ns
$\overline{G1O}$ to GD disable time	t_{65}	Write cycle 9/	9, 10, 11	01		60	ns
PCLK to INTA high time	t_{67}	INTA cycle	9, 10, 11	01		25	ns
INTA hold time	t_{68}		9, 10, 11	01	0		ns
$\overline{G1O}$ high time	t_{69}	7/ 10/	9, 10, 11	01	52		ns

1/ All testing to be performed using worst-case test conditions unless otherwise specified.
2/ Devices supplied to this drawing will meet all levels M, D, L, R and F of irradiation. However, this device is only tested at the 'F' level. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.
3/ Go/No Go test. There are no recorded measurements.
4/ Measurement is made with the RAM sense AMPS disabled.
5/ ICCOP increases with frequency.
6/ These parameters are given for application purposes and are required for proper operation. The test value measured must be less than the specifed minimum or greater than the specified maximum.
7/ Tested with $t_1 = t_1$ (min). For $t_1 > t_1$ (min), add $t_1 - t_1$ (min) to this parameter.
8/ If CYCEXT and/or ARCE bit is set, add 1 x t_1 (min) to this parameter for USER memory access (CYCEXT case), or external ASIC bus read (ARCE case).
9/ Tested with t_1 at specified minimum and $t_2 = 0.5 \times t_1$. For $t_2 > 0.5 \times t_1$(min) add $t_2 - (0.5 \times t_1(\text{min}))$ to this parameter.
10/ If ARCE bit is set, add 1 x t_1(min) to this parameter for external ASIC read cycles.

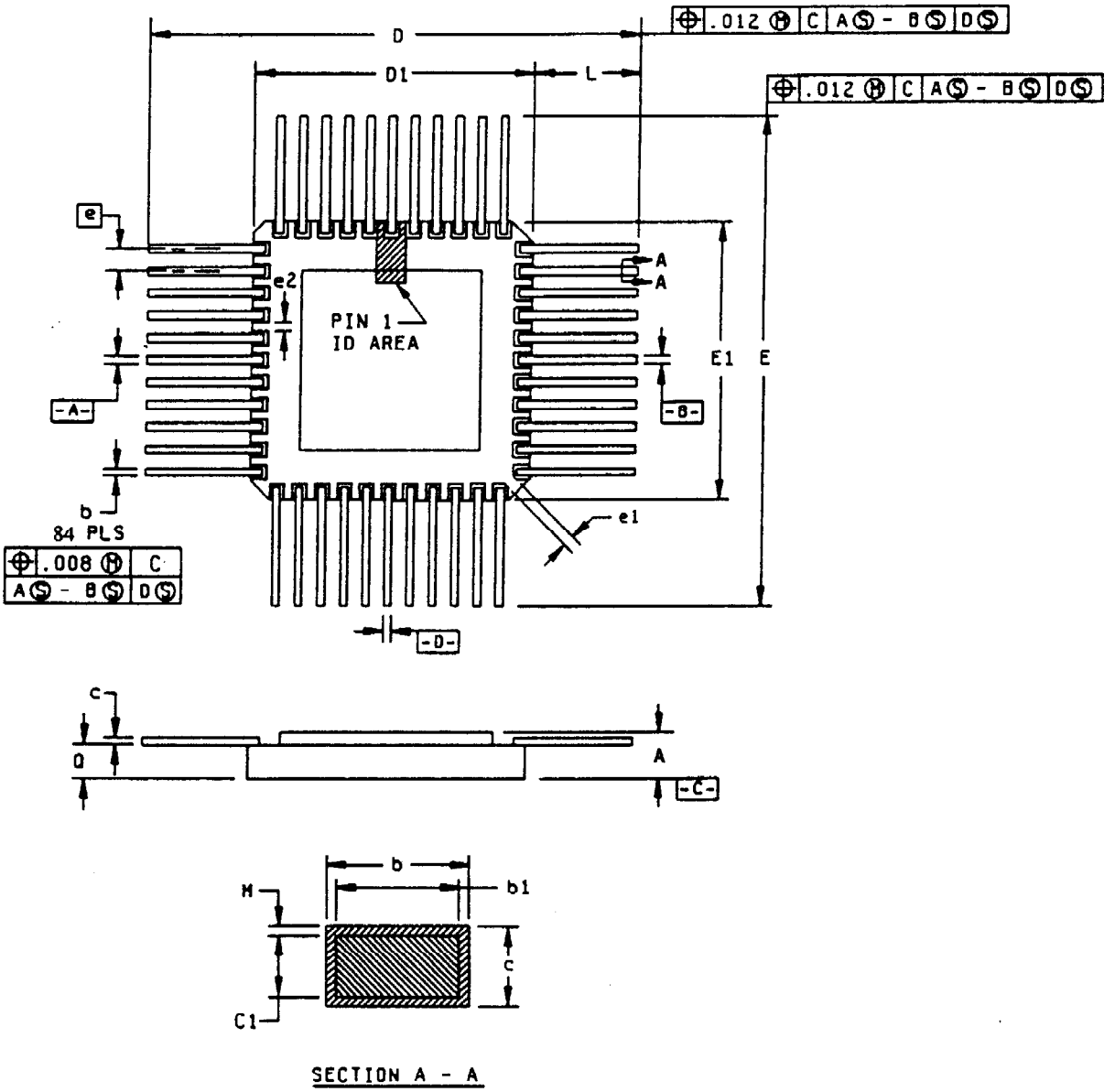


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-95635
		REVISION LEVEL	SHEET 10

Symbol	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	-	2.67	-	0.105	
b	0.38	0.56	0.015	0.022	2
b1	0.38	0.48	0.015	0.019	2
c	0.20	0.38	0.008	0.015	2
c1	0.20	0.30	0.008	0.012	2
D	45.72	50.80	1.800	2.000	
E	45.72	50.80	1.800	2.000	
D1	28.83	29.72	1.135	1.170	
E1	28.83	29.72	1.135	1.170	
e	1.27 BSC		0.050 BSC		
e1	0.30	-	0.012	-	4
e2	0.30	-	0.012	-	
L	8.13	11.43	0.320	0.450	
Q	1.78	2.29	0.070	0.090	6
M	-	0.04	-	0.0015	2
N	84		84		3

Notes:
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. N is the maximum number of terminal positions.
4. Measure dimension e1 at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimensions Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch(0.0038 mm) maximum when solder dip lead finish is applied.
7. The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and the inch-pound units the inch pound units shall take precedence.

Figure 1. Case outline - Continued

Case X

Pin	Terminal	Pin	Terminal	Pin	Terminal
A1	E15	C10	VDD	J2	GD03
A2	E13	C11	MD06	J5	MA04
A3	E12	D1	GD15	J6	MA06
A4	VDD	D2	GIO	J7	GND
A5	INTA	D10	MD05	J10	MA18
A6	TCLK	D11	GND	J11	GND
A7	GA00	E1	GND	K1	GD04
A8	MD14	E2	GD13	K2	GD02
A9	MD12	E3	GD14	K3	GD01
A10	MD11	E9	MD04	K4	MA02
A11	MD08	E10	MD03	K5	MA05
B1	ICLK	E11	MD02	K6	MA07
B2	RESET	F1	GD07	K7	MA10
B3	E14	F2	GD12	K8	MA13
B4	E11	F3	GD11	K9	MA15
B5	NMI	F9	MD00	K10	MA17
B6	GND	F10	NEW	K11	MA19
B7	MD15	F11	MD01	L1	GND
B8	MD13	G1	GD09	L2	GD00
B9	MD10	G2	GD08	L3	MA01
B10	MD09	G3	GD10	L4	MA03
B11	MD07	G9	MR/W	L5	MA06
C1	GR/W	G10	BOOT	L6	MA11
C2	WAIT	G11	PCLK	L7	MA09
C3	Alignment Pin	H1	VDD	L8	MA12
		H2	GD06	L9	VDD
C5	INTSUP	H10	LDS	L10	MA14
C6	GA02	H11	UDS	L11	MA16
C7	GA01	J1	GD05		

FIGURE 2. Terminal connections.

Case Y

Terminal	Symbol	Terminal	Symbol	Terminal	Symbol
1	GA02	30	GD04	59	UDS
2	TCLK	31	GD03	60	NEW
3	INTA	32	GND	61	BOOT
4	NMI	33	GD02	62	PCLK
5	INTSUP	34	GD01	63	MR/W
6	VDD	35	GD00	64	MD00
7	EI1	36	MA01	65	MD01
8	EI2	37	MA02	66	MD02
9	EI3	38	MA03	67	MD03
10	EI4	39	MA04	68	MD04
11	EI5	40	MA05	69	GND
12	RESET	41	MA06	70	MD05
13	WAIT	42	MA07	71	MD06
14	ICLK	43	MA08	72	MD07
15	GR/W	44	GND	73	VDD
16	GIO	45	MA09	74	MD08
17	GD15	46	MA10	75	MD09
18	GD14	47	MA11	76	MD10
19	GD13	48	MA12	77	MD11
20	GND	49	MA13	78	MD12
21	GD12	50	VDD	79	MD13
22	GD11	51	MA14	80	MD14
23	GD10	52	MA15	81	GND
24	GD09	53	MA16	82	MD15
25	GD08	54	MA17	83	GA00
26	GD07	55	MA18	84	GA01
27	VDD	56	MA19		
28	GD06	57	GND		
29	GD05	58	LDS		

FIGURE 2. Terminal connections. - Continued

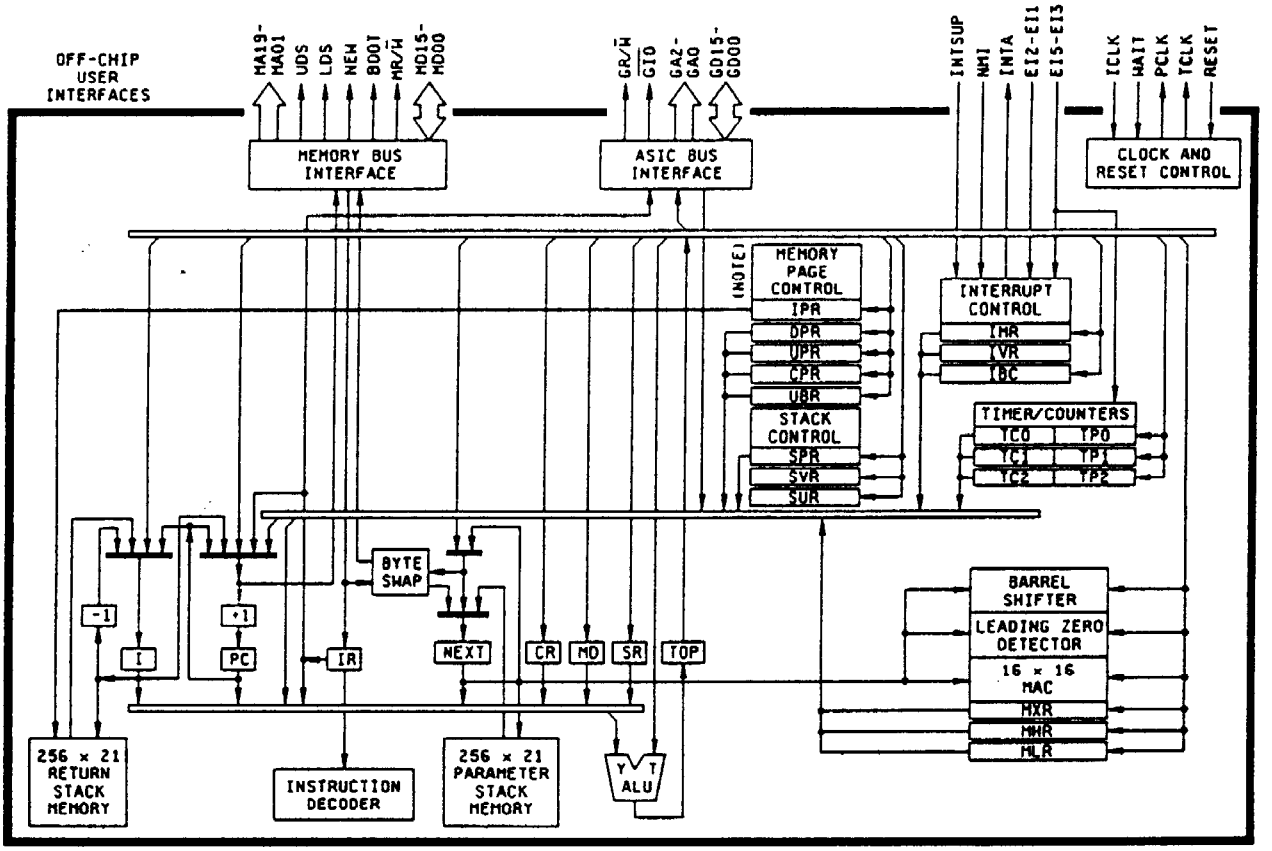
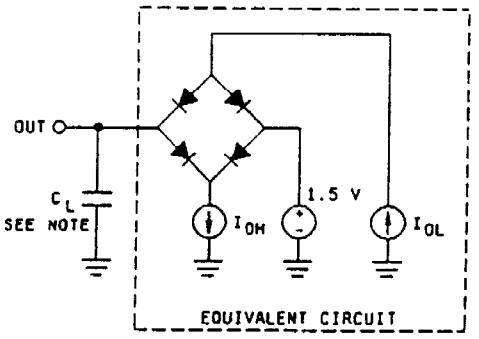
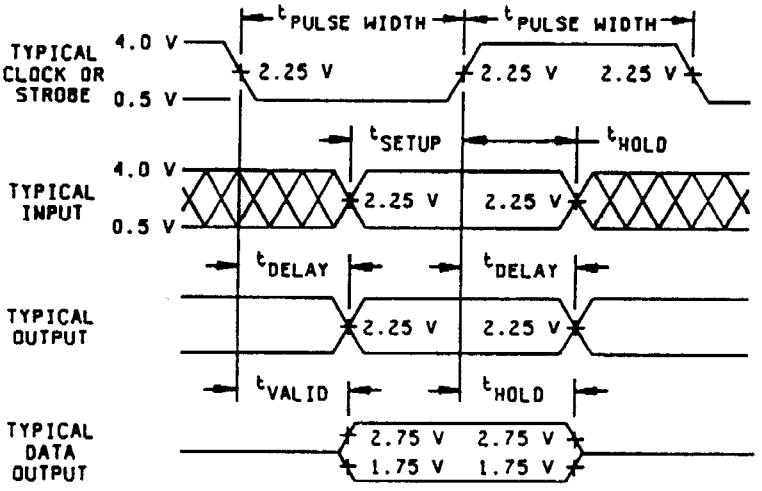


FIGURE 3. Block diagram.

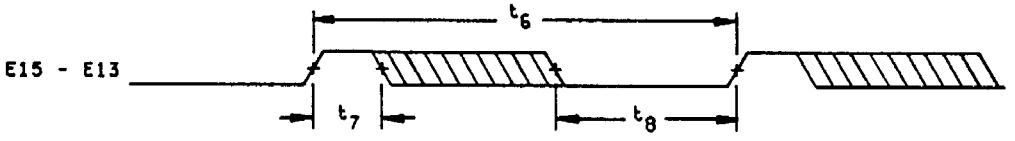


TEST CIRCUIT

Note: For AC testing input rise and fall times are driven at 1 V/ns.

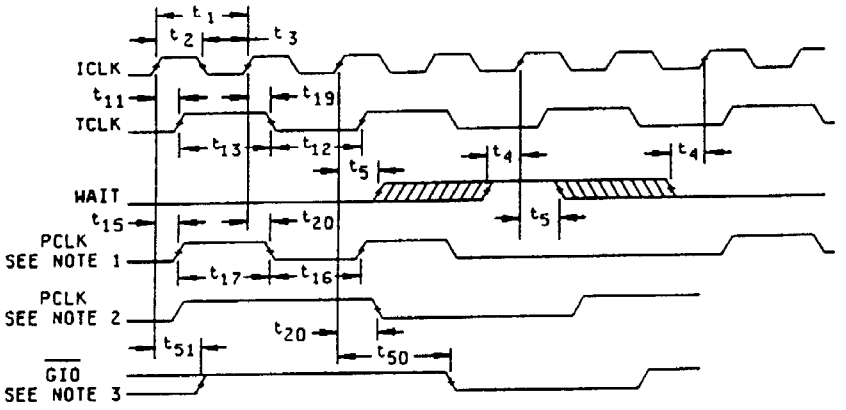


AC DRIVE AND MEASURE POINTS - CLK INPUT



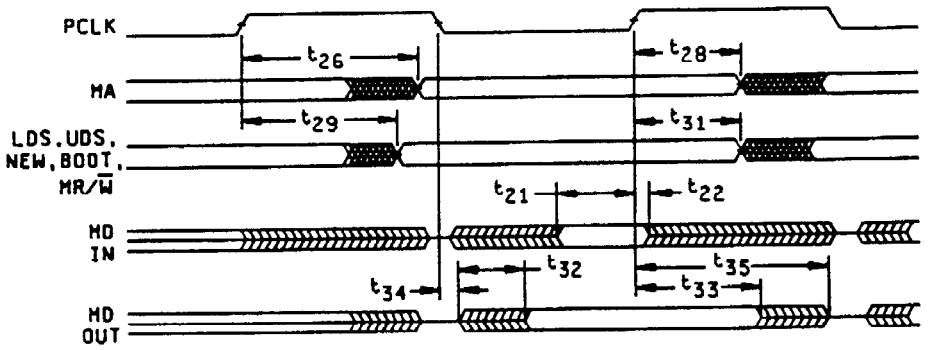
TIMER/COUNTER TIMING

Figure 4. Timing waveforms and test circuit.



CLOCK AND WAIT TIMING

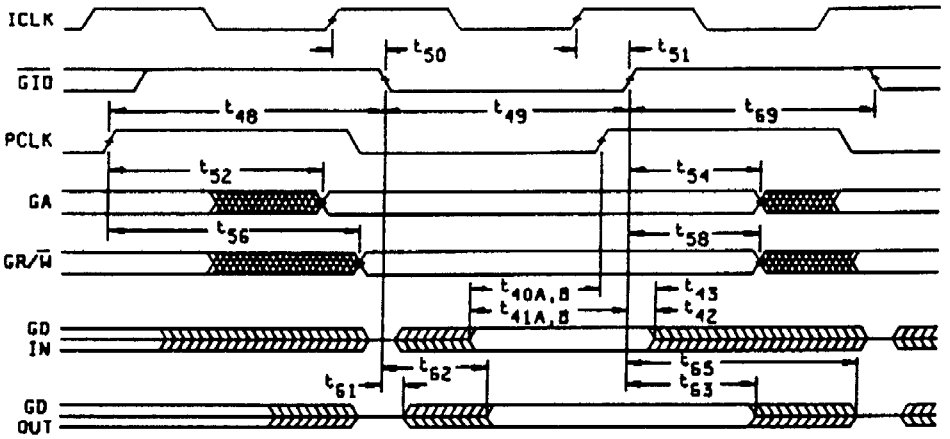
Notes:
1. Normal cycle: This waveform describes a normal PCLK cycle and a PCLK cycle with a WAIT state.
2. Extended cycle: This waveforms describes a PCLK cycle for a USER memory access or an external ASIC bus read cycle when the CYCEXT bit or ARCE bit is set.
3. Extended cycle: This waveform describes a GIO cycle for an external ASIC bus read when the ARCE bit is set.
4. An active high signal on the RESET input is guaranteed to reset the processor if its duration is greater than or equal to 4 rising edges of ICLK plus 1/2 ICLK cycle setup and hold times. If the RESET input is active for less than four rising edges of ICLK, the processor will not reset.



MEMORY BUS TIMING

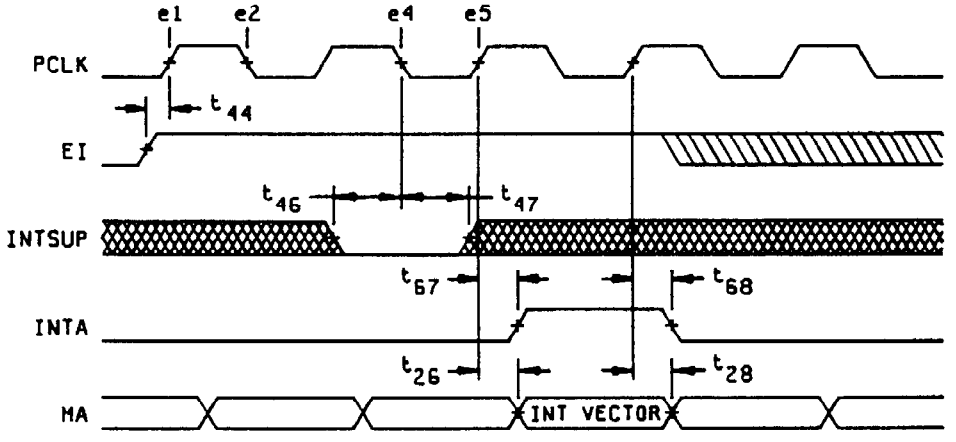
Notes:
1. If both LDS and UDS are low, no memory access is taking place in the current cycle. This only occurs during streamed instructions that do not access memory.
2. During a streamed single cycle instruction, the memory data bus is driven by the processor.

FIGURE 4. Timing waveforms and test circuits. - Continued



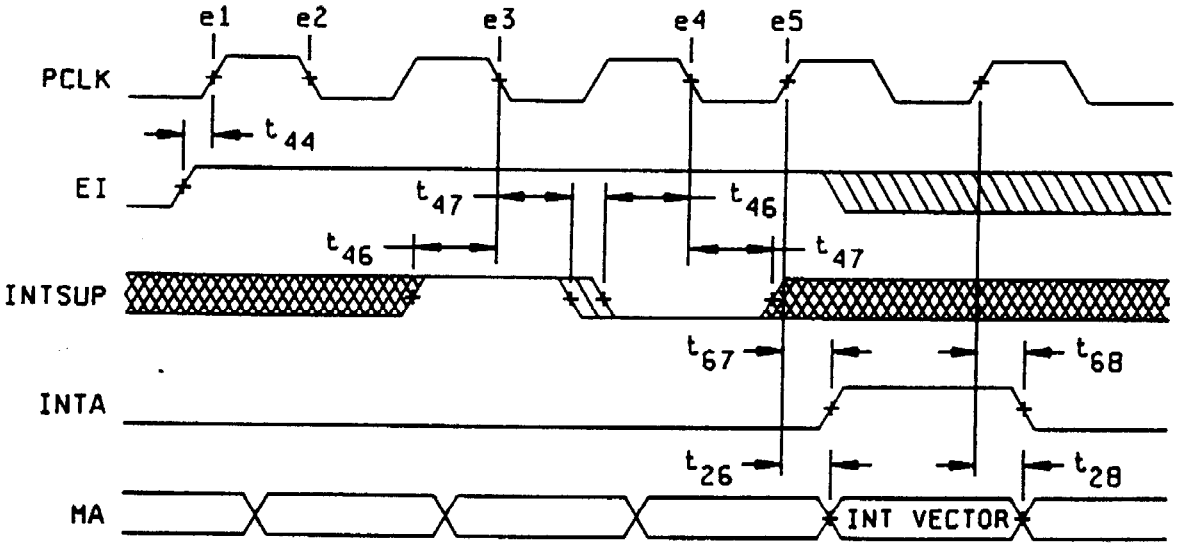
ASIC BUS TIMING

Notes:
1. GIO remains high for internal ASIC bus cycles.
2. GR/W goes low and GD is driven for all ASIC write cycles, Including internal ones.
3. During non-ASIC write cycles, GD is not driven by the device. Therefore, it is recommended that all GD pins be pulled to V_{CC} or GND to minimize power supply current and noise.
4. t40B and t41B parameters are for streamed mode of operation only.



INTERRUPT TIMING: WITH NO INTERRUPT SUPPRESSION

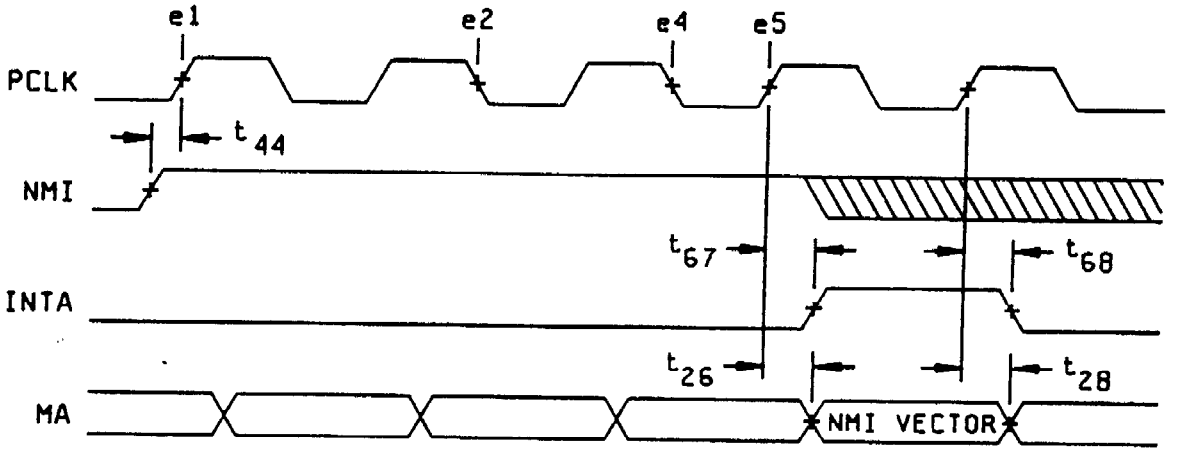
FIGURE 4. Timing waveforms and test circuits. - Continued



INTERRUPT TIMING: WITH INTERRUPT SUPPRESSION

Notes:
1. Events in an interrupt sequence are as follows:
   - e1. The interrupt controller samples the interrupt request inputs on the rising edge of PCLK. If NMI rises between event 1 and the rising edge of PCLK prior to event 5, the interrupt vector will be for NMI.
   - e2. If any interrupt request were sampled, the interrupt controller issues an interupt request to the core on the falling edge of PCLK.
   - e3. The core samples the state of the interrupt request from the interrupt controller on the falling edge of PCLK. If INTSUP is high, maskable interrupts will not be detected at this time.
   - e4. When the core samples an interrupt request on the falling edge of PCLK, an interrupt acknowledge cycle will begin on the next rising edge of PCLK.
   - e5. Following the detection of an interrupt request by the core, an interrupt acknowledge cyle begins. The interrupt vector will be based on the highest priority interrupt request active at this time.
2. t44 is only required to determine when the interrupt acknowldge cycle will occur.
3. Interrupt request should be held active until the interrupt acknowledge cycle for than interrupt occurs.

FIGURE 4. Timing waveforms and test circuits. - Continued



NON-MASKABLE INTERRUPT TIMING

Notes:
1. Events in an interrupt sequence are as follows:
   - e1. The interrupt controller samples the interrupt request inputs on the rising edge of PCLK. If NMI rising between event 1 and the rising edge of PCLK prior to event 5, the interrupt vector will be for NMI.
   - e2. If any interrupt request were sampled, the interrupt controller issues an interrupt request to the core on the falling edge of PCLK.
   - e4. When the core samples an interrupt request on the falling edge of PCLK, an interrupt acknowledge cycle will begin on the next rising edge of PCLK.
   - e5. Following the detection of an interrupt request by the core, an interrupt acknowledge cycle begins. The interrupt vector will be based on the highest priority interrupt request active at this time.
2. t44 is only required to determine when the interrupt acknowledge cycle will occur.
3. Interrupt request should be held active until the interrupt acknowledge cycle for that interrupt occurs.
4. NMI has a glitch filter which requires the signal that initiates NMI last at least two falling edges of ICLK.

FIGURE 4. Timing waveforms and test circuits. - Continued

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 or as specified in the QM plan including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) Shall be measured only for the initial test and after process or design changes which may affect capactitance. Tests shall be sufficient to validate limits as defined in Table I.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 1/ 9, 10, 11	1, 2, 3, 7, 1/ 8, 9, 10, 11	1, 2, 3, 2/3/ 7,8,9,10,11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8 9, 10, 11	1, 2, 3, 4, 7 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9 10, 11	1, 2, 3, 7, 8 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1 and 7.
2/ PDA applies to subgroups 1, 7 and delta limits.
3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see Table I).

Table IIB. Burn-in Delta Parameters (+25°C)

Parameter	Symbol	Delta limits
Standby power supply current	I_{CCSB}	±150 μA
Input leakage current	I_{IO}	±2μA
Low level output voltage	V_{OL}	±60 mV
TTL high level output voltage	V_{OH1}	±550 mV

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-I-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). SEP testing shall be required on class V devices (See 1.4). SEP testing shall be performed on a technology basis on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

Table III. Irradiation bias conditions 1/

Pin number Case Y	Resistor Value	Signal/ level	Pin number Case Y	Resistor value	Signal/ Level	Pin number Case Y	Resistor Value	Signal/ level
1	47kΩ	V_{DD}	30	47kΩ	V_{DD}	59	47kΩ	GND
2	47kΩ	V_{DD}	31	47kΩ	V_{DD}	60	47kΩ	GND
3	47kΩ	V_{DD}	32		GND	61	47kΩ	GND
4	47kΩ	GND	33	47kΩ	V_{DD}	62	47kΩ	V_{DD}
5	47kΩ	V_{DD}	34	47kΩ	V_{DD}	63	47kΩ	GND
6		V_{DD}	35	47kΩ	V_{DD}	64	47kΩ	V_{DD}
7	47kΩ	GND	36	47kΩ	V_{DD}	65	47kΩ	V_{DD}
8	47kΩ	GND	37	47kΩ	V_{DD}	66	47kΩ	V_{DD}
9	47kΩ	GND	38	47kΩ	V_{DD}	67	47kΩ	V_{DD}
10	47kΩ	GND	39	47kΩ	V_{DD}	68	47kΩ	V_{DD}
11	47kΩ	GND	40	47kΩ	V_{DD}	69		GND
12	47kΩ	GND	41	47kΩ	V_{DD}	70	47kΩ	GND
13	47kΩ	GND	42	47kΩ	V_{DD}	71	47kΩ	V_{DD}
14	47kΩ	V_{DD} 2/	43	47kΩ	V_{DD}	72	47kΩ	GND
15	47kΩ	GND	44		GND	73		V_{DD}
16	47kΩ	GND	45	47kΩ	V_{DD}	74	47kΩ	GND
17	47kΩ	V_{DD}	46	47kΩ	V_{DD}	75	47kΩ	GND
18	47kΩ	V_{DD}	47	47kΩ	V_{DD}	76	47kΩ	V_{DD}
19	47kΩ	V_{DD}	48	47kΩ	V_{DD}	77	47kΩ	GND
20		V_{DD}	49	47kΩ	V_{DD}	78	47kΩ	V_{DD}
21	47kΩ	V_{DD}	50		V_{DD}	79	47kΩ	V_{DD}
22	47kΩ	V_{DD}	51	47kΩ	V_{DD}	80	47kΩ	V_{DD}
23	47kΩ	V_{DD}	52	47kΩ	V_{DD}	81		GND
24	47kΩ	V_{DD}	53	47kΩ	V_{DD}	82	47kΩ	V_{DD}
25	47kΩ	V_{DD}	54	47kΩ	V_{DD}	83	47kΩ	V_{DD}
26	47kΩ	V_{DD}	55	47kΩ	V_{DD}	84	47kΩ	V_{DD}
27		V_{DD}	56	47kΩ	V_{DD}			
28	47kΩ	V_{DD}	57		GND			
29	47kΩ	V_{DD}	58	47kΩ	GND			

1/ V_{DD} = 5.5 V.
2/ Apply a minimum of $10I_{CLK}$.

Table III. Irradiation bias conditions - Continued 1/

Pin number Case X	Resistor Value	Signal/ level	Pin number Case X	Resistor value	Signal/ Level	Pin number Case X	Resistor Value	Signal/ level
C6	47kΩ	V_{DD}	K1	47kΩ	V_{DD}	H11	47kΩ	GND
A6	47kΩ	V_{DD}	J2	47kΩ	V_{DD}	F10	47kΩ	GND
A5	47kΩ	V_{DD}	D11		V_{DD}	G10	47kΩ	GND
B5	47kΩ	GND	K2	47kΩ	V_{DD}	G11	47kΩ	V_{DD}
C5	47kΩ	V_{DD}	K3	47kΩ	V_{DD}	G9	47kΩ	GND
A4		V_{DD}	L2	47kΩ	V_{DD}	F9	47kΩ	V_{DD}
B4	47kΩ	GND	L3	47kΩ	V_{DD}	F11	47kΩ	V_{DD}
A3	47kΩ	GND	K4	47kΩ	V_{DD}	E11	47kΩ	V_{DD}
A2	47kΩ	GND	L4	47kΩ	V_{DD}	E10	47kΩ	V_{DD}
B3	47kΩ	GND	J5	47kΩ	V_{DD}	E9	47kΩ	V_{DD}
A1	47kΩ	GND	K5	47kΩ	V_{DD}	J7		GND
B2	47kΩ	GND	L5	47kΩ	V_{DD}	D10	47kΩ	GND
C2	47kΩ	GND	K6	47kΩ	V_{DD}	C11	47kΩ	V_{DD}
B1	47kΩ	V_{DD}	J6	47kΩ	V_{DD}	B11	47kΩ	GND
C1	47kΩ	GND	E1		GND	L9		V_{DD}
D2	47kΩ	GND	L7	47kΩ	V_{DD}	A11	47kΩ	GND
D1	47kΩ	V_{DD}	K7	47kΩ	V_{DD}	B10	47kΩ	GND
E3	47kΩ	V_{DD}	L6	47kΩ	V_{DD}	B9	47kΩ	V_{DD}
E2	47kΩ	V_{DD}	L8	47kΩ	V_{DD}	A10	47kΩ	GND
B6		V_{DD}	K8	47kΩ	V_{DD}	A9	47kΩ	V_{DD}
F2	47kΩ	V_{DD}	H1		V_{DD}	B8	47kΩ	V_{DD}
F3	47kΩ	V_{DD}	L10	47kΩ	V_{DD}	A8	47kΩ	V_{DD}
G3	47kΩ	V_{DD}	K9	47kΩ	V_{DD}	L1		GND
G1	47kΩ	V_{DD}	L11	47kΩ	V_{DD}	B7	47kΩ	V_{DD}
G2	47kΩ	V_{DD}	K10	47kΩ	V_{DD}	A7	47kΩ	V_{DD}
F1	47kΩ	V_{DD}	J10	47kΩ	V_{DD}	C7	47kΩ	V_{DD}
C10		V_{DD}	K11	47kΩ	V_{DD}			
H2	47kΩ	V_{DD}	J11		GND			
J1	47kΩ	V_{DD}	H10	47kΩ	GND			

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331 and Table IV.

Table IV. Pin descriptions

Signal	Description
	OUTPUTS
NEW	NEW: A High on this pin indicates that an instruction fetch is in progress.
BOOT	BOOT: A high on this pin indicates that Boot Memory is being accessed. This pin can be set or reset by accessing bit 3 of the coniguration register.
MR/W	Memory Read/Write: A low on this pin indicates that a memory write operation is in progress.
UDS	Upper Data Select: A high on this pin indicates that the high byte of memory (MD15-MD08) is being accessed.
LDS	Lower Data Select: A high on this pin indicates that the low byte of memory (MD07-MD00) is being accessed.
GIO	ASIC I/O: A low on this pin indicates that an ASIC bus operation is in progress.
GR/W	ASIC Read/Write: A low on this pin indicates that an ASIC bus write operation is in progress
PCLK	Processor Clock: Runs at half the frequency of ICLK. All processor cycles begin on the rising edge of PCLK. Held low extra cycles when WAIT is asserted.
TCLK	Timing Clock: Same frequency and phase as PCLK but continues running during Wait cycles.
INTA	Interrupt acknowledge: A high on this pin indicates that an interrupt acknowledge cycle is in progress.
	INPUT
WAIT	WAIT: A high on this pin casuses PCLK to be held low and the current cycle to be extended.
ICLK	Input Clock: Internally divided by 2 to generate all on-chip timing (CMOS input levels).

Symbol	Description
RESET	RESET: A high on this pin resets the device. Must be held high for at least 4 rising edges of ICLK plus 12 ICLK cycles setup and hold times.
EI2, EI1	External interrupts2, 1: Active high level-sensitive inputs to the interrupt controller. Sampled on the rising edge of PCLK.
EI5-EI3	External interrupts 5, 4, 3: Dual purpose inputs; active high level-sensitive interrupt controller inputs; active high edge-sensitive timer/counter inputs. As interrupt inputs, they are sampled on the rising edge of PCLK.
NMI	NON-Maskable Interrupt: Active high edge-sensitive interrupt controller input capable of interrupting any processor cycle when NMI is set to Mode 0.
INTSUP	Interrupt supress: A high on this pin inhibits all maskable interrupts, internal and external.
GA00-GA02	Asic address: 3-bit ASIC address bus, which carries information for external ASIC devices.
MA01-MA19	Memory address: 19-bit memory address bus, which carries address information for main memory.
GD00-GD15	ASIC data: 16-bit bidirectional external ASIC data bus, which carries data to and from off-chip I/O devices.
MD00-MD15	Memory data: 16-bit bidirectional memory data bus, which carries data to and from main memory.
V_{DD}	Power supply +5 V connections. A 0.1 μF, low impedance decoupling capacitor should be placed between V_{DD} and GND. This should be located as close to the package as possible.
GND	Power supply ground return connections.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

6.8 Additional information. A copy of the following additional data shall be maintained and available from the approved source of supply.

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 95-09-27

Approved sources of supply for SMD 5962-95635 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962F9563501QXC	34371	HS8-RTX2010RH-8
5962F9563501QYC	34371	HS9-RTX2010RH-8
5962F9563601VXC	34371	HS8-RTX2010RH-Q
5962F9563501VYC	34371	HS9-RTX2010RH-Q

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Harris Semiconductor P O Box 883 Melbourne FL 32902-0883